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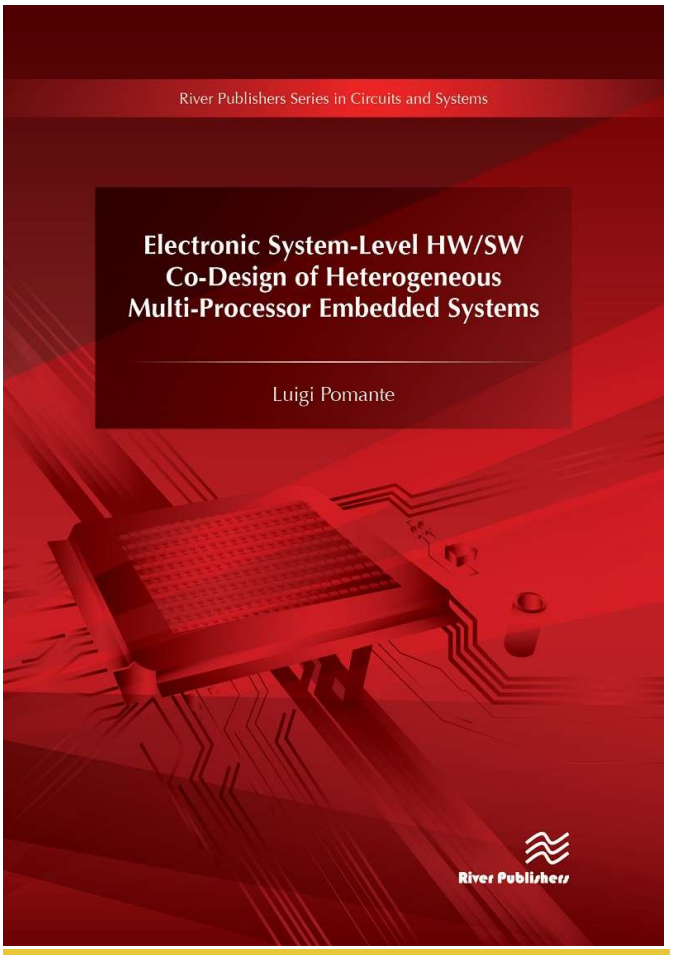
Electronic System-Level HW/SW Co-Design of Heterogeneous Multi-Processor Embedded Systems

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Modern electronic systems consist of a fairly heterogeneous set of components. Today, a single system can be constituted by a hardware platform, frequently composed of a mix of analog and digital components, and by several software application layers. The hardware can include several heterogeneous microprocessors (e.g. GPP, DSP, GPU, etc.), dedicated ICs (ASICs and/or FPGAs), memories, a set of local connections between the system components, and some interfaces between the system and the environment (sensors, actuators, etc.). Therefore, on the one hand, multi-processor embedded systems are capable of meeting the demand of processing power and flexibility of complex applications. On the other hand, such systems are very complex to design and optimize, so that the design methodology plays a major role in determining the success of the products. For these reasons, to cope with the increasing system complexity, the approaches typically used today are oriented towards co-design methodologies working at the higher levels of abstraction. Unfortunately, such methodologies are typically customized for the specific application, suffer of a lack of generality and still need a considerable effort when real-size project are envisioned. Therefore, there is still the need for a general methodology able to support the designer during the high-level steps of a co-design flow, enabling an effective design space exploration before tackling the low-level steps and thus committing to the final technology. This should prevent costly redesign loops.

In such a context, the work described in this book, composed of two parts, aims at providing models, methodologies and tools to support each step of the co-design flow of embedded systems implemented by exploiting heterogeneous multi-processor architectures mapped on distributed systems, as well as fully integrated onto a single chip.

The first part focuses on issues like the analysis of system specification languages, and the analysis of existing system-level HW/SW co-simulation methodologies to support heterogeneous multi-processor architectures. The second part focuses mainly on Design Space Exploration, and it presents both some theoretical advancements with respect to the first part, and the development of a prototypal framework that provides practical exploitation of the proposed concepts.



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